



INFORMATION DISCLOSURE STATEMENT

Applicant : Li, et al.
App. No. : 10/614,622
Filed : July 7, 2003
For : METHODS OF INCREASING WRITE
SELECTIVITY IN AN MRAM
Examiner : H. Jey Tsai
Group Art Unit : 2812

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed is form PTO-1449 listing four (4) references. Copies of disclosed U.S. patents and/or publications are not included pursuant to PTO waiver of the requirement under 37 C.F.R. § 1.98(a)(2)(i) for applications filed after June 30, 2003. Copies of other references, if listed, are enclosed.

This Information Disclosure Statement is being filed with an RCE, and no fee is required in accordance with 37 C.F.R. § 1.97 (b)(4). Identification herein is not an admission that any of the foregoing references are prior art to the above-captioned application.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: March 19, 2004

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FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
MICRON.198C1DV1APPLICATION NO.
10/614,622INFORMATION DISCLOSURE STATEMENT
BY APPLICANT

(USE SEVERAL SHEETS IF NECESSARY)

APPLICANT
Li, et al.FILING DATE
July 7, 2003GROUP
2812

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
	6,104,633	8/15/00	Abraham, et al.			Feb. 10, 1998
	6,134,139	10/17/00	Bhattacharyya, et al.			Jul. 28, 1999

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

EXAMINER
INITIAL

OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	M. Durlam, et al. "A low power 1Mbit MRAM based on 1T1MTJ bit cell integrated with Copper Interconnects," 2002 Symposium on VLSI Circuits, Digest of Technical Papers (IEEE June 2002), pp. 158-161.
	M. Durlam, et al., "A 0.18 μ m 4Mb Toggling MRAM," 2003 IEEE International Electron Devices Meeting, IEDM 2003 Technical Digest (IEEE 2003), pp. 995-997.

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EXAMINER

DATE CONSIDERED

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